XA-9485A
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

First Named Inventor: MURANAKA, MASAYA Art Unit: 2114

Appln. No.: 10/808,285 Examiner: Bonura

Filed: March 25, 2004 Conf. No.: 5094

For: METHOD OF DECIDING ERROR RATE AND SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

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AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action of October 16, 2006, please amend the above-identified patent application as indicated below.

Amendments to the specification begin on page 2 of this paper.

Amendments to the claims are reflected in the listing of claims which begins on page 3 of this paper.

Amendments to the drawings begin on page 6 of this paper.

Remarks begin on page 7 of this paper.